RENESAS

Operating Precaution

V850E2/Sx4-H

µPD70F4017 µPD70F4018

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Table of Contents

Cover 1

Table of Contents 2

Notice 3

Regional Information 6

Chapter 1 Introduction 7

1.1 Overview and Devices Crossreference 7

1.2 Related Documents 7

Chapter 2 Difference details 8

1. PTCTL Pin 8

2. CAN configuration 8

3. Error Counter Clearing of FCN controllers 9

3.1 Shutdown of CAN Module after reaching Initialization Mode 9

3.2 Clearing of all Pending Transmit Requests 12

3.3 Do not clear error counters except after “bus off” 14

3.4 Do not clear the error counter states at all 14

Chapter 3 Revision History 15

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Chapter 1 Introduction

1.1 Overview and Devices Crossreference

appl.: precaution is applicable to this device

not appl.: precaution is not applicable to this device

Outline	μPD70F4017 μPD70F4018	
	DS 1.0	
1. PTCTL Pin (Technical limitation)	appl.	
2. CAN configuration (Direction of Use)	appl.	
3. Error Counter Clearing of FCN controllers (Direction of Use)	appl.	

1.2 Related Documents

This Operating Precaution is complementary to the following documents:

Document Title	Document No.	Date published
V850E2/Sx4-H Preliminary Hardware User's Manual	R01UH0107EJ0001, Rev. 0.01	2011-02-10

Chapter 2 Difference details

1. PTCTL Pin

Description (A) It is not possible to use the PTCTL pin (PTCTL is used to control an external power transistor to supply 1.2 V to CVDD).

(B) Current consumption may be increased by up to 1.8 mA in DEEPSTOP mode.

Workaround (A) Supply 1.2 V to CVDD by an external regulator which is not controlled by PTCTL1.

(B) There is no workaround.

2. CAN configuration

Description When configuring the FCN module one of the following combinations for

- the supplied clock for FCN f_{CAN},
- the CAN baudrate and
- the number of timequantas (TQ) per data bit time (DBT)

must be used:

CAN baudrate [kbps]	Supplied clock for FCN f_{CAN} [MHz]	TQs per DBT
1000	16	8
1000	24	8
1000	32	8
1000	40	≤10
500	16	≤16
500	20	≤10
500	24	≤12
500	32	≤16
500	40	≤20
250	16	≤16
250	20	≤20
250	24	≤24
250	32	≤16
250	40	≤20

Note The table describes common combinations. For other combinations please contact your local Renesas engineering representative.

Workaround There is no workaround.

3. Error Counter Clearing of FCN controllers

Description In applications, which are clearing the error counter status during run-time, use one of the following procedure recommendations:

Notes
1. The error counters referred to in this document are located in the registers FCNnCMINSTR, FCNnCMERCNT.
2. The Clear Error Counter flags referred to in this document are located in the FCNnCMCLERCF bits

3.1 Shutdown of CAN Module after reaching Initialization Mode

If FCN is shut down and re-started, after the initialization mode has been reached, all error counter states are cleared anyway. In addition, this also serves as a procedure to avoid any unexpected behaviour situation.

Follow the sequence below in strict oder from (a) to (c).

(a) Set the FCNnGMCLCLOM flag to clear the FCNnGMCLPWOM global operation mode bit.

Caution Confirm the clearance by reading back. If unsuccessful, use the forced shutdown by setting the FCNnGMCLESDE in advance.

(b) Re-start the CAN controller by setting the FCNnGMCLSEOM bit.

Note This leads back to initialization mode, with all error counter states cleared.

(c) Restore the register settings of the CAN module configuration.

The following register settings must be restored, because they are reset to their initial values, when the CAN module was shut down.

- FCNnGMADCTL
- FCNnCMMKCTLx
- FCNnCMCLCTL
- FCNnCMIECTL
- FCNnCMBRPRS
- FCNnCMBTCTL
- FCNnCMTSCTL
- Registers of all message buffers

Notes
1. The interrupt status flags of FCNnCMISCTL are cleared and cannot be restored.

2. The contents of the history lists are cleared and cannot be restored.
3. All message buffer contents need not to be restored, even though following flags must be cleared.
   - FCNnMmCTL.FCNnMmDTNF
   - FCNnMmCTL.FCNnMmTRQF

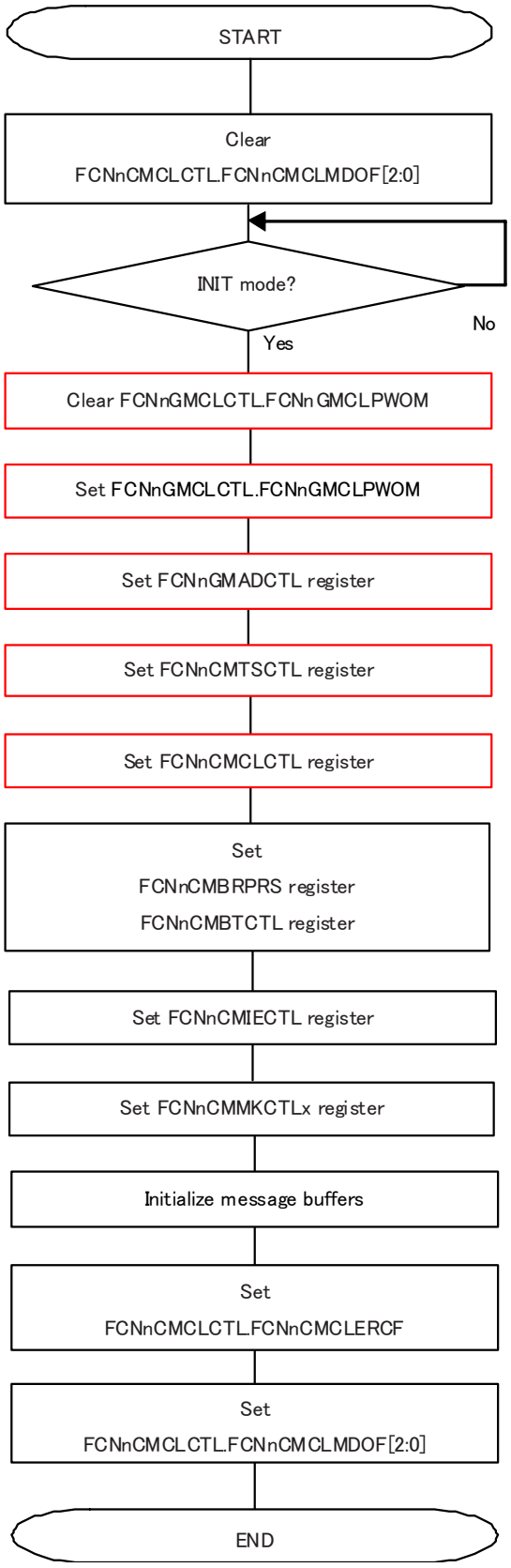

Figure 2-1 Shutdown and restart of CAN Module to clear Error Counters of FCN

3.2 Clearing of all Pending Transmit Requests

Follow the sequence below in strict oder from (a) to (c).

Before entering the initialization mode of FCN always:

(a) Clear any pending ABT mode trigger.

Caution Confirm the clearance and stopping of the ABT operation by reading the FCNnGMABCTL.FCNnGMABABTT flag.

(b) Clear all transmit requests by software.

Cautions
1. Any flag “FCNnMmTRQF” must be cleared.
2. Clearing of “FCNnMmTRQF” must be confirmed by reading back.

(c) Wait on transmission completion by 11 CAN bits and cleared Transmission Status Flag.

Caution Confirm the transmission completion by waiting for 11 CAN bits and check that the transmission status flag FCNnCMCLSSTS is not set after that. This is according to a recommended transmission abort processing flow.

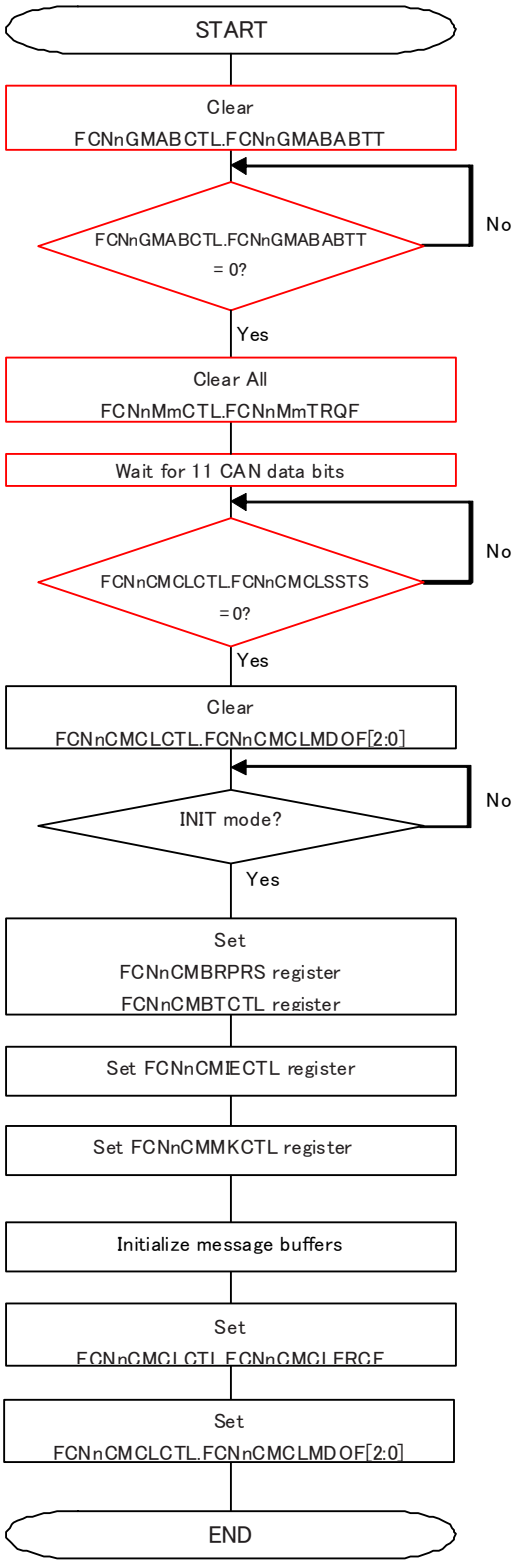

Figure 2-2 Clearing of Transmit Requests for FCN before clearing Error Counters

3.3 Do not clear error counters except after “bus off”

In “bus off” state, the operating precaution is not applicable. Therefore, there is no restriction in usage of the FCNnCMCLERCF when the CAN controller is in “bus off” state.

Note The “bus off” state can be determined by reading the FCNnCMINBOFF.

3.4 Do not clear the error counter states at all

According to ISO, this approach is recommended.

Like this, a node will behave according to the ISO 11898 specification. The behaviour of a node during “bus off” and the behaviour of restoring of the “error passive” state of a node are the impacts of this procedure. If the error counters are not cleared, the penalties of the ISO specification for erroneous nodes will become active, which are typically resulting in degraded performance on the CAN bus, until the node has recovered to “error active” state.

Chapter 3 Revision History

Version	Date	Change description
1.0	2011-04-01	Initial version
2.0	2011-05-12	Added item 2: “CAN configuration” and item 3: “Error Counter Clearing of FCN/DCN controllers”.
3.0	2011-06-27	Modified document number for official release.

Renesas Electronics Europe

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